

## **UCD30xx System Module (SYS) Programmer's Manual**

Literature Number: xxxxxx

Date

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# 1 Description

This document details the system module registers memory map as listed in Table 1. A detailed description of each register and its bits is provided. Each register begins on a word boundary.

SYS Registers have the following attributes:

- 16-bit wide
- Addresses placed on word boundaries
- Byte, half-word and word writes permitted
- All Registers can be read in any mode of operation.
- Global Control Register is writeable in privilege mode only. All other Registers are writeable in any mode.

## 2 Register Map

Address	Register Name	Description	Bits	Read	Write	Reset
0xFFFF_FFD0	CLKCNTL	Clock Control Register	10	Yes	Yes	10'h0
0xFFFF_FFE0	SYSECR	System Exception Control Register	16	Yes	Yes	16'h4000
0xFFFF_FFE4	SYSESR	System Exception Status Register	16	Yes	No	16'h0
0xFFFF_FFE8	ABRTESR	Abort Exception Status Register	16	Yes	No	16'h0
0xFFFF_FFEC	GLBSTAT	Global Status Register	8	Yes	No	8'h0
0xFFFF_FFF0	DEV	Device Identification Register	16	Yes	No	16'h187F
0xFFFF_FFF8	SSIF	System Software Interrupt Flag	1	Yes	No	1'h0
0xFFFF_FFFC	SSIR	System Software Interrupt Request	16	Yes	Yes	16'h0

Table 1 Register Map

## 3 Register Description

### 3.1 Clock Control Register (CLKCNTL)

#### Address FFFFFFFD0

The first 2 bits of clock control Register can be used to slow down the processor clock to reduce the processor power consumption. This register also configures SYNC\_OUTPUT pin, please refer to “UCD30xx General Purpose Input Output (GPIO) Programmer’s Manual” and “UCD30xx Fusion Digital Power Peripherals Programmer’s Manual” for related information. CLKCNTL is accessible in user and privilege mode and supports byte, half-word and word accesses. Any access to this Register takes two SYSCLK cycles.

Bit Number	9:8	7	6:5	4	3	2:0
Bit Name	M_DIV_RATIO	RESERVED	CLKSR	CLKDIR	CLKDOUT	RESERVED
Access	-	-	R/W	R/W	R/W	-
Default	00	0	00	0	0	000

**Bits 9-8: M\_DIV\_RATIO** – MCLK (Processor Clock) Divide Ratio

00 = MCLK frequency equals High Frequency Oscillator divided by 8 (Default)

01 = MCLK frequency equals High Frequency Oscillator divided by 16  
 10 = MCLK frequency equals High Frequency Oscillator divided by 32  
 11 = MCLK frequency equals High Frequency Oscillator divided by 64

**Bit 7: RESERVED**

**Bit 6-5: CLKSR** – These bits control the source/function of the SYNC\_OUTPUT pin.

00 = Configured as a digital input/output pin (Default)  
 01 = Driven by the interface clock (ICLK)  
 10 = Driven by the CPU clock (MCLK)  
 11 = Driven by the system clock (SYSCLK)

**Bit 4: CLKDIR** – This bit represents the SYNC\_OUTPUT pin direction.

0 = CLKOUT pin is configured as an input (Default)  
 1 = CLKOUT pin is configured as an output

**Bit 3: CLKDOUT** – This pin represents the SYNC\_OUTPUT output pin data.

0 = CLKOUT driven to logic low in output mode (Default)  
 1 = CLKOUT driven to logic high in output mode

**Bits 2-0: RESERVED**

### 3.2 System Exception Control Register (SYSECR)

**Address FFFFFFFE0**

The system exception control Register contains bits that allow the user to generate a software reset. The OVR bits disable certain reset/abort conditions when TRST is high.

Bit Number	15:14	13:3	2	1	0
Bit Name	RESET	RESERVED	PACCOVR	ACCOVR	ILLOVR
Access	R/W	-	R/W	R/W	R/W
Default	00	-	0	0	0

**Bits 15-14: RESET** – Software Reset Enable. These bits always read as 01

01 = No reset  
 1X = Global system reset (X = don't care)  
 X0 = Global system reset (X = don't care)

**Bits 13-3: RESERVED**

**Bit 2: PACCOVR** – Peripheral Access Violation Override

0 = Peripheral access violation error causes a reset or abort (Default)  
 1 = No action taken on a peripheral access violation

**Bit 1: ACCOVR** – Memory Access Reset Override

0 = Memory access violation error causes a reset or abort (Default)

1 = No action taken on an illegal address

**Bit 0: ILLOVR** – Illegal Address Reset Override

0 = Illegal address causes a reset or abort (Default)

1 = No action taken on an illegal address

### 3.3 System Exception Status Register (SYSESR)

#### Address FFFFFFFE4

The System Exception Status Register contains flags for different reset/abort sources. On power-up, all bits are cleared to 0. When a reset condition is recognized, the appropriate bit in the Register is set and the value of the bit is maintained through the reset. When a new reset condition occurs, the current contents of this Register are not cleared. The contents of this Register are cleared on a power-on reset or by software.

Bit Number	15	14	13	12	11	10
Bit Name	PORRST	RESERVED		ILLMODE	ILLADR	ILLACC
Access	R/W	-		R/W	R/W	R/W
Default	0	00		0	0	0

Bit Number	9	8	7	6:0
Bit Name	PILLACC	ILLMAP	SWRST	RESERVED
Access	R/W	R/W	R/W	-
Default	0	0	0	000_0000

**Bit 15: PORRST** – Power-On reset flag. Set when power-on reset is asserted. Reset is asserted as long as power-on-reset is active. Whenever a device is powered, this bit is set.

User and privilege modes (read)

0 = Power-up reset has not occurred since the last clear

1 = Power-up reset has occurred since the last clear

User and privilege modes (write)

0 = Clears the corresponding bit to 0

1 = No effect

**Bit 14-13: RESERVED** – Reserved for future use

**Bit 12: ILLMODE** – This bit represents the illegal mode flag. This bit is set when the mode bits in the program status Register are set to an illegal value.

User and privilege modes (read)

0 = Illegal mode has not occurred since the last clear

1 = Illegal mode has occurred since the last clear

User and privilege modes (write)

0 = Clears the corresponding bit to 0

1 = No effect

**Bit 11: ILLADR** – This bit represents the illegal address access flag. This bit is set when an access to an unimplemented location in the memory map is detected in non-user mode.

User and privilege modes (read)  
0 = Illegal address has not occurred since the last clear  
1 = Illegal address has occurred since the last clear  
User and privilege modes (write)  
0 = Clears the corresponding bit to 0  
1 = No effect

**Bit 10: ILLACC** – This bit represents the illegal memory access flag. This bit is set when an access to a protected location without permission rights is detected in non-user mode.

User and privilege modes (read)  
0 = Illegal memory access has not occurred since the last clear  
1 = Illegal memory access has occurred since the last clear  
User and privilege modes (write)  
0 = Clears the corresponding bit to 0  
1 = No effect

**Bit 9: PILLACC** – This bit represents the peripheral illegal access flag. This bit is set when a peripheral access violation is detected in user mode.

User and privilege modes (read)  
0 = Illegal peripheral access has not occurred since the last clear  
1 = Illegal peripheral access has occurred since the last clear  
User and privilege modes (write)  
0 = Clears the corresponding bit to 0  
1 = No effect

**Bit 8: ILLMAP** – This bit represents the illegal address map flag. This bit is set when the base addresses of one or more memories overlap. Reset occurs when the overlapped registration is accessed.

User and privilege modes (read)  
0 = Illegal address mapping has not occurred since the last clear  
1 = Illegal address mapping has occurred since the last clear  
User and privilege modes (write)  
0 = Clears the corresponding bit to 0  
1 = No effect

**Bit 7: SWRST** – This bit represents the software reset flag. This bit is set when the last reset is caused by software writing the RESET bits.

User and privilege modes (read)  
0 = Software reset has not occurred since the last clear  
1 = Software reset has occurred since the last clear  
User and privilege modes (write)  
0 = Clears the corresponding bit to 0  
1 = No effect

**Bit 6-0: RESERVED**

### 3.4 Abort Exception Status Register (ABRTESR)

Address FFFFFFFE8

The Abort Exception Status Register shows the abort cause.

Bit Number	15	14	13	12:0
Bit Name	ADRABT	MEMABT	PACCVIO	RESERVED
Access	R/W	R/W	R/W	-
Default	0	0	0	0_0000_0000_0000

**Bit 15: ADRABT** – This bit represents the illegal address abort. An illegal address access was detected in user mode. An abort was generated due to an illegal address access from either the MPU or system

User and privilege modes (read)

0 = No illegal address

1 = Abort caused by an illegal address

User and privilege modes (write)

0 = Clears bit to 0

1 = No effect

**Bit 14: MEMABT** – This bit represents the memory access abort. This bit indicates an illegal memory access was detected in user mode. An abort was generated due to the illegal memory access from either the MPU or system.

User and privilege modes (read)

0 = No illegal memory access

1 = Abort caused by an illegal memory access

User and privilege modes (write)

0 = Clears bit to 0

1 = No effect

**Bit 13: PACCVIO** – This bit represents the peripheral access violation error. This bit indicates a peripheral access violation error was detected during a peripheral Register access in user mode. An abort was generated due to a peripheral access violation.

User and privilege modes (read)

0 = No peripheral access violation

1 = Abort caused by a peripheral access violation

User and privilege modes (write)

0 = Clears bit to 0

1 = No effect

**Bit 12-0: RESERVED** – Unused bits

### 3.5 Global Status Register (GLBSTAT)

Address FFFFFFFEC

The Global Status Register specifies the module that triggered the illegal address, illegal access, abort or reset. When a new reset condition reset occurs, the current contents of this Register are not cleared. The contents of this Register are cleared on a power-on reset or by software.

Bit Number	7	6	5	4	3:0
Bit Name	SYSADDR	SYSACC	MPUADDR	MPUACC	RESERVED
Access	R/W	R/W	R/W	R/W	-
Default	0	0	0	0	0000

**Bit 7: SYSADDR** – This bit represents the system illegal address flag. This bit is set when the system detects an illegal address.

User and privilege modes (read)

0 = No system illegal address

1 = Abort or reset caused by a system illegal address

User and privilege modes (write)

0 = Clears bit to 0

1 = No effect

**Bit 6: SYSACC** – This bit represents the system illegal access flag. This bit is set when the system detects an illegal access.

User and privilege modes (read)

0 = No system illegal access

1 = Abort or reset caused by a system illegal access

User and privilege modes (write)

0 = Clears bit to 0

1 = No effect

**Bit 5: MPUADDR** – This bit represents the MPU illegal address flag. This bit is set when the memory protection unit detects an illegal address.

User and privilege modes (read)

0 = No MPU illegal address

1 = Abort or reset caused by a MPU illegal address

User and privilege modes (write)

0 = Clears bit to 0

1 = No effect

**Bit 4: MPUACC** – This bit represents the MPU illegal access flag. This bit is set when the MPU detects an illegal access.

User and privilege modes (read)

0 = No MPU illegal access

1 = Abort or reset caused by a MPU illegal access

User and privilege modes (write)

0 = Clears bit to 0

1 = No effect

**Bit 3-0: RESERVED**



### 3.6 Device Identification Register (DEV)

#### Address FFFFFFFF0

The Device Identification Register contains silicon revision information that is hard coded during device manufacturing. This register is read-only.

Bit Number	15:0
Bit Name	DEV
Access	R
Default	0001_0100_0111_1111

Bits 15-0: DEV – These bits represent the device identification code. This is a read only register. See the device-specific datasheet for details on the device identification code.

### 3.7 System Software Interrupt Flag Register (SSIF)

#### Address FFFFFFFF8

The System Software Interrupt Flag Register is set when a software interrupt is triggered. The flag allows the user to poll for a software interrupt.

Bit Number	0
Bit Name	SSIFLAG
Access	R/W
Default	0

**Bit 0: SSIFLAG** – This bit represents the system software interrupt flag. This bit is set when a correct SSKEY is written to the System Software Interrupt Request Register (SSIR). This bit is cleared only by software.

User and privilege modes (read)

0 = No IRQ/FIQ interrupt request has been generated since the last clear

1 = IRQ/FIQ interrupt request has been generated since the last clear

User and privilege modes (write)

0 = Clears bit to 0

1 = No effect

### **3.8      System Software Interrupt Request Register (SSIR)**

**Address FFFFFFFC**

The System Software Interrupt Request Register contains a key sequence that triggers a software interrupt request to the CIM. Also, the Register contains an 8-bit data field.

Bit Number	15:8	7:0
Bit Name	SSKEY	SSDATA
Access	R/W	R/W
Default	0000_0000	0000_0000

**Bits 15-8: SSKEY** – These bits represent the system software interrupt request key. These write-only bits are executable in both user and privilege modes. A 0x75 written to these bits initiates IRQ/FIQ interrupts. Data in this field is always read as zero.

**Bits 7-0: SSDATA** – These bits represent the system software interrupt data. The SSDATA bits provide an 8-bit field that can be used for passing messages into the system software interrupt.